REMARKS

Claims 1-11, 26, 28-30, and 32-43 are pending in the application. Claims 1, 8, 26, 30, 33, 37, and 40 are independent. By the foregoing Amendment, Applicant seeks to amend claims 1, 26, 30, and 40 and cancel claims 17-20 and 23-25. These changes are believed to introduce no new matter and their entry is respectfully requested.

Rejection of Claims 1-2, 4, 17-18, 26, and 29-30 Under 35 U.S.C. §102(b)

In paragraph 7, the Examiner rejected claims 1-2, 4, 17-18, 26, and 29-30 under 35 U.S.C. §102(b) as anticipated by U.S. Patent No 5,231,314 to Andrews (hereinafter "Andrews"). Applicant respectfully traverses the rejection.

A claim is anticipated only if each and every element of the claim is found, either expressly or inherently, in a reference. (MPEP §2131 *citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628 (Fed. Cir. 1987)). The identical invention must be shown in as complete detail as is contained in the claim. Id. *citing Richardson v. Suzuki Motor Co.*, 868 F.2d 1226,1236 (Fed. Cir. 1989)).

Amended claim 1 recites in pertinent part "a set of sense amplifiers coupled to compare an externally supplied reference voltage with the set of DC voltages; and a boundary scan register coupled to each sense amplifier in the set of sense amplifiers to interpret the comparison of the externally supplied reference voltage and the set of DC voltages." Amended claim 26 recites in pertinent part "a set of sense amplifiers coupled to compare an externally supplied reference voltage with the set of DC voltages" Amended claim 30 recites in pertinent part "comparing an external reference voltage with the set of DC voltages" Support for these amendments can be found in Applicant's Specification at page 6, last paragraph, and Figure 1.

Andrews appears to be directed to a programmable timing circuit for an IC with a TAP port. The problem addressed in Andrews is that previous factory calibration and field tuning of timing generator circuits were unsatisfactory. Andrews proposes as a solution a programmable and controllable variable timing generator circuit formed directly on the IC

being tested. That is, Andrews is directed to testing integrated circuit timing whereas embodiments of the present invention are directed to testing integrated circuit input levels. Accordingly, Applicant respectfully submits that Andrews in not properly applied to claimed invention.

Assuming for the sake of argument that Andrews is properly applied to the claimed invention, Applicant respectfully submits that Andrews fails to teach the identical invention recited in claims 1, 26, and 30 as required by MPEP §2131. As an example, Andrews fails to teach a set of sense amplifiers coupled to compare an ***externally supplied reference voltage*** with the set of DC voltages. The ramp voltage generator RAMP that the Examiner asserts provides the "reference voltage" is located on-chip in Andrew. (Column 1, lines 41-45.)

Applicant respectfully submits that because Andrews fails to teach the identical invention as required by MPEP §2131, Andrews fails to anticipate claims 1, 26, and 30 and thus claims 1, 26, and 30 are patentable over Andrews. Claims 2 and 4 properly depend from claim 1 and are thus patentable over Andrews as well. Claim 29 properly depends from claim 26 and thus also is patentable over Andrews. Claim 32 properly depends from claim 30 and thus also is patentable over Andrews. Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the rejection to claims 1-2, 4, 26, and 29-30.

Although Applicant believes that claims 17-18 are patentable as written, by the foregoing Amendment Applicant seeks to cancel claims 17-18 to render moot the rejection of them. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 17-18.

Rejection of Claims 3, 5-6, 8-11, 19-20, 23-24, 28, 32-33, and 37-38 Under 35 U.S.C. §103(a)

In paragraph 7, the Examiner rejected claims 3, 5-6, 8-11, 19-20, 23-24, 28, 32-33, and 37-38 under 35 U.S.C. §103(a) as unpatentable over Andrews in view of U.S. Patent No 6,085,345 to Taylor (hereinafter "Taylor"). Applicant respectfully traverses the rejection.

To establish a *prima facie* case of obviousness, an Examiner must show that the cited reference teaches each and every element of the claimed invention, that there is some suggestion or motivation to modify a reference to arrive at the claimed invention, and that there is some expectation of success. (MPEP §2143.) The suggestion or motivation to modify reference teachings must be found in the references relied upon (MPEP §2143.01). The modification proposed by the Examiner cannot render the cited reference unsatisfactory for its intended purpose or change the principle of operation. (MPEP §2143.01.)

Claim 8 recites in pertinent part "a ***structural tester*** coupled to the integrated circuit to apply a reference voltage to the ***inverting input*** of each sense amplifier in the set of sense amplifiers" (emphasis added). Claim 33 recites in pertinent part "a ***structural tester*** coupled to the integrated circuit to apply a reference voltage to the inverting input of each sense amplifier in the set of sense amplifiers" (emphasis added). Claim 37 recites in pertinent part "a ***structural tester*** coupled to the integrated circuit to apply a reference voltage to the ***inverting input*** of each sense amplifier in the set of sense amplifiers" (emphasis added).

Applicant respectfully reiterates that Andrews is not properly applied to the claimed invention because Andrews is directed to testing integrated circuit timing whereas embodiments of the present invention are directed to testing integrated circuit input levels. Applicants respectfully submit further that Taylor does not make up for the deficiency because Taylor also is not properly applied to the claimed invention. For example, Taylor appears to be directed to timing control for input/output testability for source synchronous inputs whereas embodiments of the present invention are directed to testing integrated circuit input levels.

Assuming for the sake of argument that Andrews and Taylor are properly applied to the claimed invention, Applicant respectfully submits that the Examiner points to no motivation or suggestion in Andrews or Taylor themselves to combine Andrews and Taylor to arrive at the claimed invention, for example, testing integrated circuit input levels. This is because Andrews in view of Taylor in further view of Bates are directed to timing tests not input levels testing.

In the Office Action, the Examiner concedes that Taylor fails to teach "a structural tester coupled to the integrated circuit to apply a reference voltage to the inverting input of the sense amplifier" but asserts that because Andrews teaches a ramp generator RAMP connected to the STS input through boundary scan cells of the boundary scan register TDR1 and because Taylor suggests that circuitry can be externally controlled by a logic tester during testing through the boundary scan logic that it would have been obvious to one of ordinary skill in the art that a structural tester could be added to Andrews STS pin in order to apply reference signals.

Applicant respectfully submits that the Examiner's characterization of the ramp generator RAMP in Andrews as equivalent to the reference voltage source 106 is in error. Applicant respectfully submits that the ramp generator RAMP is not equivalent to the reference voltage generator 106 in embodiments of the claimed invention because, for example, the reference voltage generator 106 is external to the integrated circuit 104 whereas the ramp voltage generator RAMP is located on-chip in Andrews. Modifying Andrews as proposed by the Examiner would make Andrews unsatisfactory for its intended purpose, which is to provide a programmable and controllable variable timing generator circuit ***formed directly on the IC being tested***. (Column 1, lines 41-45.) This rationale is prohibited under MPEP §2143.01 as a basis for rejecting the claimed invention.

Applicant respectfully submits further that Andrews in view of Taylor fails to teach each and every element of the claimed invention. For example, Applicant respectfully submits that Andrews in view of Taylor fails to teach or suggest "a ***structural tester*** coupled to the integrated circuit to apply a ***reference voltage***" as recited in claims 8, 33, and 37. Taylor appears to teach externally controlling timing delay (*see*, for example, column 5, lines 50-52 "External control with the logic tester allows the ***time to be varied*** at which the delayed strobe signal ... reaches the data latch 34"). Nowhere in Taylor or Andrews is a ***structural tester*** coupled to the integrated circuit to apply a ***reference voltage*** taught or suggested.

Applicant respectfully submits that because Andrews in view of Taylor fails to teach the each and every element of the claims 8, 33, and 37 as required by MPEP §2143, and/or an improper rationale was used in rejecting claims 8, 33, and 37, Andrews in view of Taylor do not render obvious claims 8, 33, and 37 and claims 8, 33, and 37 thus are patentable over Andrews in view of Taylor. Claims 9-11 properly depend from claim 8 and are thus patentable over Andrews in view of Taylor as well. Claim 32 properly depends from claim 30 and thus also is patentable over Andrews in view of Taylor. Claim 38 properly depends from claim 37 and thus also is patentable over Andrews in view of Taylor. Claims 3 and 5-6 properly depend from patentable claim 1 and thus also are patentable over Andrews in view of Taylor. Although Applicant believes that claims 19-20 and 23-24 are patentable as written, by the foregoing Amendment Applicant seeks to cancel claims 19-20 and 23-24 to render moot the rejection of them. Claim 28 properly depends from patentable claim 26 and thus also is patentable over Andrews in view of Taylor. Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the rejection to claims 3, 5-6, 8-11, 19-20, 23-24, 28, 32-33, and 37-38.

Rejection of Claims 7, 25, 33-36, and 39-43 Under 35 U.S.C. §103(a)

In paragraph 7, the Examiner rejected claims 7, 25, 33-36, and 39-43 under 35 U.S.C. §103(a) as unpatentable over Andrews in view of Taylor in further view of U.S. Patent No 6,584,591 to Bates et al. Applicant respectfully traverses the rejection.

Applicant respectfully points out that U.S. Patent No 6,584,591, which the Examiner refers to as "Bates" is to Taylor rather than to Bates. In the present Paper, Applicant will assume the Examiner intended to reject claims 33-36, and 39-43 under 35 U.S.C. §103(a) as unpatentable over Andrews in view of Taylor in further view of U.S. Patent No 6,477,674 to Bates et al. (hereinafter "Bates"), which Patent No. is provided on the Notice of References Cited included in the Office Action. Applicant respectfully traverses the rejection.

Claim 33 recites in pertinent part "a structural tester coupled to the integrated circuit to apply a reference voltage to the inverting input of each sense amplifier in the set of sense amplifiers" (emphasis added). Amended claim 40 recites in pertinent part "coupling a set of

levels generating circuits to a set of sense amplifiers, wherein the set of sense amplifiers are to compare ***an external reference voltage*** to a set of direct current (DC) voltage levels generated by the set of levels generating circuits; and coupling the set of sense amplifiers to input/output loop back compare circuitry to interpret the comparison of the ***external reference voltage*** and the set of voltage levels" (emphasis added).

Applicant respectfully reiterates that Andrews in view of Taylor is not properly applied to the claimed invention because Andrews is directed to testing integrated circuit timing whereas embodiments of the present invention are directed to testing integrated circuit input levels. Applicants respectfully submit further that Bates does not make up for the deficiency because Bates also is not properly applied to the claimed invention. For example, Bates appears to be directed to performing timing tests using I/O loopback whereas embodiments of the present invention are directed to testing integrated circuit input levels. I/O loopback-based tests may not be suitable for testing integrated circuit input levels because there is no mechanism to change the amplitude of input levels and/or because an output level defect may be hidden by an input level defect.

Assuming for the sake of argument that Andrews, Taylor, and Bates are properly applied to the claimed invention, Applicant respectfully submits that the Examiner points to no motivation or suggestion in Andrews, Taylor, or Bates themselves to be combined to arrive at the claimed invention, for example, testing integrated circuit input levels. This is because Andrews in view of Taylor in further view of Bates are directed to timing tests.

Applicant respectfully submits that because Andrews in view of Taylor in further view of Bates is improperly applied to the claimed invention, fails to teach the each and every element of the claims 33 and 40 as required by MPEP §2143, and/or an improper rationale was used in rejecting claims 33 and 40, Andrews in view of Taylor in further view of Bates do not render obvious claims 33 and 40 and claims 33 and 40 thus are patentable over Andrews in view of Taylor in further view of Bates. Claim 7 properly depends from claim 1 and is thus patentable over Andrews in view of Taylor in further view of Bates as well. Claim 32 properly depends from claim 30 and thus also is patentable over Andrews in

view of Taylor in further view of Bates. Although Applicant believes that claim 25 is patentable as written, by the foregoing Amendment Applicant seeks to cancel claim 25 to render moot the rejection of it. Claims 34-36 properly depend from claim 33 and thus also are patentable over Andrews in view of Taylor in further view of Bates. Claim 39 properly depends from claim 37 and thus also is patentable over Andrews in view of Taylor in further view of Bates. Claims 41-43 properly depend from claim 40 and thus also are patentable over Andrews in view of Taylor in further view of Bates. Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the rejection to claims 3, 5-6, 8-11, 19-20, 23-24, 28, 32-33, and 37-38.

CONCLUSION

Applicant submits that all grounds for rejection have been properly traversed, or rendered moot, and that the application is now in condition for allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 7/8/2004

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